CLAIMS

I claim:

1. A method of forming a contact structure for a ferroelectric memory device integrated in a semiconductor substrate and including a matrix array of ferroelectric memory cells, wherein each cell includes a MOS device connected to a ferroelectric capacitor; said MOS device having first and second conduction terminals and being covered with an insulating layer; and said ferroelectric capacitor having a lower plate formed on said insulating layer above said first conduction terminal and coupled to said first conduction terminal, and said lower plate being covered with a layer of a ferroelectric material and coupled capacitively to an upper plate, the method comprising:

forming a first plurality of plugs by forming a first plurality of openings in the insulating layer, the first plurality of openings extending from the first conduction terminals to the lower plates of the ferroelectric capacitors, lining the first plurality of openings with a conductive material, and filling the first plurality of openingswith a non-conductive material; and

forming a second plurality of plugs by forming a second plurality of openings in the insulating layer, the first plurality of openings extending from the second conduction terminals, lining the second plurality of openings with a conductive material, and filling the second plurality of openings with a conductive material.

2. The method of claim 1 wherein said first plurality of plugs are formed before forming the second plurality of plugs.

3. The method of claim 2 wherein said second plurality of plugs are formed after the ferroelectric capacitors are formed.

4. The method of claim 1 wherein said conductive material used to fill the second plurality of plugs comprises tungsten.

5. The method of claim 1 wherein said conductive material used to fill the second plurality of plugs comprises polysilicon.

6. A contact structure according to claim 1 wherein said second plurality of plugs are formed after completing said ferroelectric capacitors.

7. A method of making a non-volatile memory cell integrated in a semiconductor substrate, comprising:

forming first and second conduction terminals of a MOS transistor in the substrate and forming a gate terminal of the MOS transistor on a gate dielectric on the substrate;

covering the MOS transistor with an insulating layer;

forming a first contact plug through the insulating layer, the first contact plug being electrically connected to the first conduction terminal;

forming a capacitor having a lower plate formed on said insulating layer above said first conduction terminal and connected electrically to said first conduction terminal by the first contact plug, said lower plate being covered with a layer of a material and coupled capacitively to an upper plate; and

forming a second contact plug in the insulating layer and filled with a conductive material after completion of said capacitor, the second contact plug being electrically connected to said second conduction terminal.

8. The method of claim 7 wherein said conductive material comprises tungsten.

9. The method of claim 7 wherein said conductive material comprises polysilicon.

10. The method of claim 7 wherein said conductive material is a first conductive material and forming the second contact plug includes forming an opening in the

insulating layer and lining the opening with a second conductive material before filling the opening with the first conductive material.

11. The method of claim 7 wherein forming the first conductive plug includes forming an opening in the insulating layer, lining the opening with a conductive material, and filling the opening with a non-conductive material.

12. The method of claim 7 wherein the insulating layer is a first insulation layer, the method further comprising:

forming a second insulating layer on the capacitor, wherein the second conductive plug is formed through the second insulating layer; and

forming a metal connection layer on the second insulating layer and in contact with the second conductive plug.

13. The method of claim 7 wherein the capacitor is ferroelectric in that the layer covering the lower plate is a ferroelectric layer.

14. A method of forming a ferroelectric memory cell, the method comprising:

forming a MOS transistor having first and second terminals;

forming an insulating layer;

forming a first contact region by forming in the insulating layer a first contact opening having an interior surface, coating the interior surface of the first contact opening with a barrier layer of conductive material that contacts the first terminal, and filling the first contact opening with a non-conductive plug;

forming a second contact region by forming in the insulating layer a second contact opening having an interior surface, coating the interior surface of the second contact opening with a barrier layer of conductive material that contacts the second terminal, and filling the second contact opening with a conductive plug;

forming a ferroelectric capacitor having first and second plates, wherein the first plate is electrically connected to one of the first and second contact regions and the second plate is capacitively coupled to the first plate.

15. The method of claim 14 wherein the first plate is connected to the first contact region and the second contact region is connected to a bit line that extends above the ferroelectric capacitor.

16. The method of claim 14 wherein the barrier material for the first and second contact regions includes titanium.

17. The method of claim 14 wherein the non-conductive plug includes silicon oxide.

18. The method of claim 14 wherein the conductive plug includes tungsten.

19. The method of claim 14 wherein the second contact is formed after forming the ferroelectric capacitor.